REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 are active in this application; Claims 1-6 having been amended by the present Amendment.

In the outstanding Office Action Claims 1-6 were rejected under 35 USC §102(b) as being anticipated by Applicant admitted prior art (AAPA) shown in Figs. 5B and 6.
In light of the outstanding rejection, the claims have been amended to clarify features believed to be more clearly patentably define over the prior art. To that end, amended Claim 1 clarifies that the claimed nonvolatile semiconductor memory device according to a first aspect of the present invention includes a semiconductor substrate having an array region, on which a memory cell is formed, and a peripheral region, on which a high-voltage transistor is formed, and that according to a first aspect of the present invention, a dummy pattern is formed adjacent to the high-voltage transistor in the peripheral region, the height of the top surface of the gate insulator in the high-voltage transistor is equal to the height of the top surface of the gate insulator in the dummy pattern, the thickness of the gate insulator of the dummy pattern is equal to the thickness of the gate insulator of the high-voltage transistor, and the thickness of each gate insulator of the high-voltage transistor and the dummy pattern is greater than the thickness of the gate insulator of a memory cell formed in the array region.

Amended Claim 3 clarifies that in a nonvolatile semiconductor memory device according to a second aspect of the present invention, a guard ring is formed between the memory cell and the high-voltage transistor, the height of the top surface of the gate insulator in the high-voltage transistor is equal to the height of the top surface of the gate insulator in the guard ring, the thickness of the gate insulator of the guard ring is equal to the thickness of

the gate insulator of the high-voltage transistor, and the thickness of each gate insulator of the high-voltage transistor and the guard ring is greater than the thickness of the gate insulator of the memory cell.

Amended Claim 5 clarifies that in a nonvolatile semiconductor memory device according to a third aspect of the present invention, a guard ring is formed between the memory cell and the high-voltage transistor, a dummy pattern is formed adjacent to the high-voltage transistor, the high-voltage transistor, the guard ring and the dummy pattern have an equal height of the top surface of the gate insulator, the thickness of each gate insulator of the guard ring and the dummy pattern is equal to the thickness of the gate insulator of the high-voltage transistor, and the thickness of each gate insulator of the high-voltage transistor, the dummy pattern and the guard ring is greater than the thickness of the gate insulator of the memory cell.

Applicants respectfully traverse the outstanding rejection under 35 U.S.C. 102(b) insofar as it may be applicable to the amended claims, on the basis the AAPA only discloses that the thickness of each gate insulator of the dummy pattern and the guard ring is equal to the thickness of the gate insulator of the memory cell, and the thickness of the gate insulator of the high-voltage transistor is greater than the thickness of each gate insulator of the memory cell, the guard ring and the dummy pattern. The AAPA does not disclose at all the above three aspects of the present invention.

In light of this distinction, it is respectfully submitted that the amended claims patentably define over the AAPA and are in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

I:\ATTY\EHK\AMEND-RESPONSES\0039\23S\239969US-AM1.DOC